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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,713	03/18/2004	Chao-Hsiang Yang	67,200-967	7508

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EXAMINER	
MONDT, JOHANNES P	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/804,713	YANG, CHAO-HSIANG	
	Examiner	Art Unit	
	Johannes P. Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/18/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the Application on 3/18/2004.

Information Disclosure Statement

The examiner has considered the items listed on the Information Disclosure Statement (IDS) filed on 3/18/2004. A signed copy of Form PTO-1449 is herewith enclosed. However, Applicant is kindly requested to review item AC for possible typographical error: the specification refers to Ying as US Patent 6,330,252, which does not exist; instead there is a US Patent 6,300,252 matching substantially the description. If Applicant had intended to include said US Patent to Ying Applicant could file a supplemental IDS. For the record at this time, the examiner has considered both 6,330,252 (irrelevant) and 6,300,252 (at least closely related art).

Specification

1. The disclosure is objected to because of the following informalities: the reference to Ying et al, US Patent 6,330,252 is in error: 6,330,252 is to Shojima and appears unrelated to the application's subject matter. There is a patent to Ying et al, with patent number 6,300,252 that matches the description. Applicant should correct the reference to a non-existing patent.

Appropriate correction is required.

Claim Objections

1. ***Claim 10*** is objected to because of the following informalities: the wording "each of face" (line 2) should be replaced by "both an upper main face and a lower main face". Appropriate correction is required.

2. ***Claim 18*** is objected to because of the following informalities: the wording "each face" (line 2) should be replaced by: "both an upper main face and a lower main face". Appropriate correction is required

Double Patenting

1. ***Claim 27*** is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 22. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. ***Claim 20*** recites the limitation "each second metal layer" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. ***Claims 1-5*** are rejected under 35 U.S.C. 102(b) as being anticipated by Kagiwata (6,433,406 B1). Kagiwata teaches (title, abstract and Figures 3-5; cols. 5-8): a semiconductor device comprising: a substrate 1 (col. 5, l. 52); a top intermetal dielectric layer 3 (col. 5, l. 50) on said substrate; at least two top metal lines 4 and 5 (col. 5, l. 60-61) in said top inter-metal dielectric layer; a fuse 2 (col. 5, l. 49-52) on said top intermetal dielectric layer, said fuse in electrical communication with at least one of said at least two top metal lines (with both; see Figures 3-5); and a protective layer 10a/10b (Figure 5) on said fuse.

On claim 2: said protective layer on said fuse comprises a dielectric layer (both 10a and 10b are dielectric layers: col. 8, l. 10-33).

*On claim 3:*said dielectric layer through 10a comprises silicon dioxide (col. 8, l. 23).

On claim 4: said fuse comprises aluminum (col. 5, l. 52-53).

On claim 5: Kagiwata teaches as conventional art (Figures 1A – 2D) a semiconductor device comprising: a substrate 101 (col. 1, l. 20-24); a top inter-metal dielectric layer 109 (col. 1, l. 35-36) on said substrate; at least two top metal lines 106 and 107, respectively, (col. 1, l. 29-40) in said top inter-metal dielectric layer; a fuse 102 (col. 1, l. 29-40) *in* a top portion of said top inter-metal dielectric layer, said fuse in electrical communication with at least one of said at least two top metal lines; and a protective layer 110 (col. 1, l. 38-39) on said fuse; wherein Kagiwata teaches as

conventional as well that said at least two top metal lines comprises copper (col. 5, l. 50-54).

3. ***Claims 14-15*** are rejected under 35 U.S.C. 102(b) as being anticipated by Kajita et al (JP02001093981 A). Kajita et al teach a semiconductor device including a fuse comprising a first layer 5 comprising a copper island 5 and a second layer 6f overlying the first layer, and wherein the second layer comprises aluminum (see English Abstract and Drawing 2h.

On claim 15: the semiconductor device further comprises a dielectric layer 9 overlying the fuse (see Description of the Drawings).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. ***Claims 6-9 and 22*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kagiwata (6,433,406 B1) in view of Kajita et al (JP02001093981 A). Kagiwata teaches as conventional art (title, abstract, Figures 1-2, cols. 1-3 and col. 5, l. 49-53) a semiconductor device comprising an interconnected metallization structure 106/107 comprising copper or aluminum (col. 5, l. 49-53) and a low dielectric material (portion of 109 surrounding the structure 106/107) (col. 1, l. 35-36) surrounding the structure, and a fuse 102 (col. 1, l. 29-33) comprising copper or aluminum connected to the structure. *Kagiwata does not necessarily teach* the interconnected metallization structure to

comprise copper and the fuse to comprise aluminum. *However, it would have been obvious* to include said further limitation in view of Kajita et al, who, in a patent on a semiconductor device with a fuse (see title and English abstract), - hence closely related to the art of Kagiwata, teach to select said two top metal lines to comprise copper (see English Abstract, "Solution") while forming the fuse of aluminum (loc.cit.) so as to prevent fuse material to diffuse into the semiconductor device, in particular transistors on the substrate. *Motivation* to include the teaching by Kajita derives from the application also of Kagiwata to transistors, being part of DRAMs (col. 1 of Kagiwata). *Combination* merely involves a particular sub-selection of materials already recommended by Kagiwata (see Kagiwata, col. 5, l. 49-54).

On claim 7: the semiconductor device further comprises a dielectric layer 10a/10b (col. 8, l. 11-32) overlying the fuse.

On claim 8: said dielectric layer 10a/1`0b comprises silicon dioxide (through 10a (col. 8, l. 24-26).

On claim 9: the structure by Kagiwata further includes a first metal layer 104 and topmost metal layer (top-most layer 104) (see Figure 1D or Figure 2D) and further comprising an inter-metal dielectric layer (portion of 109 comprising low-dielectric material interposed between the first and second metal layers) interposed between the first metal layer and the second metal layer of the structure.

On claim 11: the semiconductor device further comprises a plug 105 (col. 1, l. 57-59) extending between the first metal layer and the topmost metal layer of the structure.

6. ***Claim 10*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kagitawa and Kajita et al as applied to claim 10 above, and further in view of Ying et al (6,300,252 B1). As detailed above, claim 9 is unpatentable over Kagiwata in view of Kajita et al, neither necessarily teaching the further limitation as defined by claim 10. However, the term "etch stop layer" in the present context of the device invention contains functional language to the extent in which purpose for etching rather than material constitution is indicated by said term. Applicant is reminded in this regard that in reference to the claim language, such as in the present claim, referring to "etch stop", intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963). For this reason patentable weight is only given to the term "etch stop layer" for the material constitution implied by the term in view of the specification (page 11, discussing silicon nitride layer 54 as "etch stop" layer), and not for the purpose of providing an etch stop. In this context it would have been obvious to include silicon nitride layers on each upper and lower face of said inter-metal dielectric layer (said portion of 109 comprising low-k dielectric material interposed between said first and second metal layers) in view of Ying et al, who, in a patent on etching fuse windows for a semiconductor device (title and abstract), hence closely related art, teach to include a silicon nitride layer 72 (col. 6, l. 55-63) on an upper main face of low-k dielectric layer 60/66/70 (TEOS, e.g.) (note that 60/66/70 does

comprise said low-k dielectric material interposed between metal layers M1, M2 or M3 on the one hand and M4 on the other hand) so as to prevent moisture penetration (col. col. 6, l. 63) and a silicon nitride layer 54 on a lower main face of said low-k dielectric layer so as to function as an etch stop layer (col. 6, l. 18-26). *Motivation* to include the teaching by Ying et al in this regard derives immediately from the generic undesirability of moisture as conducting material in a fuse for layer 72 and from the need to conduct an etching step (as described in Ying in col. 7, l. 35-40) also in Kagiwata (col. 7, l. 8-17).

7. ***Claim 12*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kagiwata and Kajita et al as applied to claim 6 above, and further in view of Admitted Prior Art by Applicant. Neither Kagiwata nor Kajita et al necessarily disclose a thickness or thickness range for said aluminum fuse. However, it would have been obvious to include the further limitation on the range of the thickness of the fuse in view of Admitted Prior Art by Applicant (page 3), who teach a range between 500 Å and 5000 Å, which range overlaps with the range as claimed (1000-7000 Å). Applicant is reminded that it has been held that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

8. ***Claim 13*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kagiwata and Kajita et al as applied to claim 9 above, and further in view of Liaw (6,255,715). As detailed above, claim 9 is unpatentable over Kagiwata in view of Kajita

et al, neither necessarily teaching the further limitation as defined by claim 13. *However, it would have been obvious to include said further limitation in view of Liaw et al,* who, in a patent on a fuse with guard ring for a semiconductor device or integrated circuit (title, abstract and col. 1, l. 5-18), hence closely related to the art of Kagiwata, teach the thickness of the topmost metal layer 54 to be in the range of between about 2000 and 8000 Å (col. 6, l. 25-30). *Applicant is reminded* that it has been held that a *prima facie* case of obviousness typically exists when the ranges as claimed overlap the ranges disclosed in the prior art or when the ranges as claimed do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

9. ***Claims 16-17 and 19-21*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kajita et al in view of Kagiwata (6,433,406). As detailed above, Kajita et al anticipate claim 15. Kajita et al do not necessarily teach the further limitation that said dielectric layer to comprise silicon dioxide (*claim 16*) nor the further limitation defined by *claim 17*. However, it would have been obvious to include said further limitation of claim 16 in view of Kagiwata, who, in a patent on a semiconductor device with fuse (abstract), hence closely related art, teach the selection of silicon dioxide for the material of a dielectric layer 10a overlying the fuse 2 (Figure 5, col. 8, l. 11-29) so as to avoid stress between the fuse and said dielectric layer (loc.cit.). *Motivation* to include the teaching by Kajita et al derives from the advantage thus obtained of improved mechanical strength of the semiconductor device with fuse (loc.cit.).

Furthermore, it would have been obvious to include the further limitation as defined by claims 17 and 20 in view of Kagiwata who teaches as conventional art the inclusion of a guard ring comprising first metal layer 104 and topmost metal layer 104, - and with a plug extending among each metal layer(claim 20; thus providing added mechanical rigidity), and further comprising an inter-metal dielectric layer 109 comprising a low dielectric material 109 interposed between the first metal layer and topmost metal layer, so as to form a guard ring to prevent moisture penetration (col. 1, l. 54-65 and col. 3, l. 32-37). *Motivation* to include the teaching by Kagiwata in this regard derives at least from the deleterious effects of moisture on electrical integrity known by those of ordinary skills in the art and from the added rigidity through the use of plugs.

Furthermore, it would have been obvious to include said further limitation defined by claim 19 in view of Kagiwata who teaches a first passivation layer 110 (col. 1, l. 37-39) to overlie the topmost layer, so as to function as the uppermost layer of the structure on the substrate thus providing added protection.

Finally, the fuse window (*claim 21*) formed through the passivation layer down to the fuse, said passivation layer overlying the fuse, is in evidence in Kagiwata and immediately flows from the design by Kagiwata to enable the fuse to be blown through a laser beam (cf. col. 1C and 1D and col. 1, l. 54-65).

10. ***Claim 18*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kajita et al and Kagiwata as applied to claim 17 above, and further in view of Ying et al (6,300,252 B1). As detailed above, claim 17 is unpatentable over Kajita et al in view of Kagiwata, neither necessarily teaching the further limitation defined by claim 18.

However, the term "etch stop layer" in the present context of the device invention contains functional language to the extent in which purpose for etching rather than material constitution is indicated by said term. Applicant is reminded in this regard that in reference to the claim language, such as in the present claim, referring to "etch stop", intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963). For this reason patentable weight is only given to the term "etch stop layer" for the material constitution implied by the term in view of the specification (see, for instance, page 11, discussing silicon nitride layer 54 as "etch stop" layer), and not for the purpose of providing an etch stop. In this context it would have been obvious within the context of the combined invention of Kajita et al and Kagiwata as defined above to include silicon nitride layers on each upper and lower face of said inter-metal dielectric layer (said portion of 109 in Kagiwata comprising low-k dielectric material interposed between said first and second metal layers) in view of Ying et al, who, in a patent on etching fuse windows for a semiconductor device (title and abstract), hence closely related art, teach to include a silicon nitride layer 72 (col. 6, l. 55-63) on an upper main face of low-k dielectric layer 60/66/70 (TEOS, e.g.) (note that 60/66/70 does comprise said low-k dielectric material interposed between metal layers M1, M2 or M3 on the one hand and M4 on the other hand) so as to prevent moisture penetration (col. col. 6, l. 63) and a silicon nitride layer

54 on a lower main face of said low-k dielectric layer so as to function as an etch stop layer (col. 6, l. 18-26). *Motivation* to include the teaching by Ying et al in this regard derives immediately from the generic undesirability of moisture as conducting material in a fuse for layer 72 and from the need to conduct an etching step (as described in Ying in col. 7, l. 35-40) also in Kagiwata (col. 7, l. 8-17).

11. ***Claims 22-27*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kagiwata, Kajita et al and Pricer et al (6,335,229 B1) (see IDS).

On claims 22 and 27 (see objection to claim 27 made above): The semiconductor device defined by the above-stated combination of Kagiwata and Kajita et al as delineated above can be used and is advocated to be used (Kagiwata col. 1, l. 40-55 and Figure 1D) as a method of blowing a fuse in a semiconductor device including at least a first metallization layer 106/107comprising copper (through the specific teaching by Kajita et al), and a fuse comprising aluminum (again through the specific teaching by Kajita et al as explained overleaf in this section). Neither Kagiwata nor Kajita et al necessarily limit the range of the wavelength as claimed; however, directing a laser beam onto the fuse using a wavelength ranging from 300-500 or 1000-1400 nm. However, as shown by Pricer et al, a range between 150 nm and 400 nm is conventional for blowing fuses through low-k dielectric material (col. 4, l. 47-56). Applicant is reminded that it has been held that a *prima facie* case of obviousness typically exists when the ranges as claimed overlap the ranges disclosed in the prior art or when the ranges as do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d

1379 (CA FC 2003). In the underlying case said ranges clearly and substantially overlap.

On claim 23: the semiconductor device further includes a passivation layer 110 (col. 1, l. 37-39) overlying the fuse.

On claim 24: Kagiwata further teaches that the inclusion of a silicon dioxide layer between a silicon nitride layer and the fuse reduces the mechanical stress between said fuse and said silicon nitride layer (col. 8, l. 11-33), thus improving the mechanical strength in comparison with conventional art. Motivation stems from said improvement of mechanical stress and consequently greater mechanical integrity.

On claims 25-26: However, it would have been obvious to include said further limitation in view of Kajita et al, who, in a patent on a semiconductor device with a fuse (see title and English abstract), - hence closely related to the art of Kagiwata, teach to select said two top metal lines to comprise copper, each forming a copper island (see English Abstract, "Solution") while forming the fuse of a first layer of aluminum (loc.cit.) so as to prevent fuse material to diffuse into the semiconductor device, in particular transistors on the substrate (claim 25); alternatively the copper island defined above can be considered part of the fuse, thus meeting claim 26, as then the second layer is above-mentioned first layer of aluminum. *Motivation* to include the teaching by Kajita derives from the application also of Kagiwata to transistors, being part of DRAMs (col. 1 of Kagiwata). *Combination* merely involves a particular sub-selection of materials already recommended by Kagiwata (see Kagiwata, col. 5, l. 49-54).

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Kagiwata (US 2003/0011042 A1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
July 8, 2005

Patent Examiner:

Johannes Mondt (Art Unit: 2826).